Advertisement for the JRF position in the SERB-DST Sponsored Project

Applications are invited from eligible candidates for the position of Junior Research Fellow (JRF) in a sponsored research project funded by the Science and engineering research board (SERB), Ministry of Science and Technology, Government of India, under the supervision of Dr. Abhishek Acharya. The duration of the position is a maximum of three years. The selected candidate may have the opportunity to register in the Ph.D. program as per institute norms. The details of the project are mentioned below:

Title of the project	**Design and Characterization of Radiation Hardened Standard Cell Library using Nanosheet Field Effect Transistors: Improving on Design Margins/Reliability**
Name & address of sponsoring agency	Science and Engineering Research Board (SERB), DST, Govt. of India, New Delhi
Name of the post	JRF
No. of post	01
Duration	One year, extendable upto three years or till project ends
Principal Investigator	Dr. Abhishek Acharya, Department of Electronics Engineering, Sardar Valllabhbhai National Institute of Technology Surat-395007 (Gujarat)
Essential Qualification	First Class M.E. /M.Tech. in VLSI & Microelectronics, VLSI & Embedded Systems, Electronics Engineering, Electronics & Communication Engineering, or related Allied branches. Candidate having experience/specialization in the field of above mentioned project and qualified GATE, will be given preference.
Desirable Qualification	Background in Microelectronics & VLSI Design
Fellowship	Rs. 31000/- (pre-revised), as per the SERB-JRF/SRF norms
How to apply	A soft copy of the scanned application form with supporting documents may be sent via email **abhishek@eced.svnit.ac.in** on or before **20-04-2024**. Original documents, including age proof, certificates, degrees, mark sheets, and other testimonials, must be presented at the time of the interview.
Important Dates	• Last Date to Apply (Online document): 20 April 2024, 05:00 PM. • Last date to receive application in Physical Mode: 25 April 2024, 05.00 PM. • Display of eligible candidates list on Institute Website: 29 April 2024 • Tentative date of interview/ test: 2nd week of May 2024 **(Exact schedule will be communicated through email / institute website).**
Address of Correspondence	Abhishek Acharya, Associate Professor Department of Electronics Engineering, Sardar Vallabhbhai National Institute of Technology Surat Ichchhanath, Dumas Road - 395007, Gujarat, India

Interested candidates are required to note the following:

1. The interested candidates will be required to submit their application form along with all essential details and scanned copy of all their original certificates, mark sheets and a recent passport size photograph by the last date, *i.e*, 20/04/2024, 05:00 PM. For submission of offline application (see Annexure-I), fill all the necessary details and the application with all enclosures should reach the address specified above by 25/04/2024, 05.00 PM.
2. Candidates need to bring the complete hardcopy set of the application form with xerox copies of all required documents on the day of interview for verification purpose.
3. Candidates are required to positively mention their e-mail ID and Mobile Number in the Application Form.
4. The applications received within the last date & time stipulated will be screened by a selection committee, and a list of eligible candidates shortlisted for interview/test will be displayed on the Institute's official website along with the date and time schedule of the interview/test. The Screening Committee will devise its own criteria for shortlisting of candidates for interview. Merely fulfilling main eligibility criteria may not be suitable for eligible to be invited for the interview/test.
5. The decision of SVNIT-Surat in all matters relating to eligibility, acceptance, screening, mode of selection will be final and binding on the candidates and no enquiry correspondence will be entertained in this connection from any individual or any agency on behalf of the candidate.
6. The original documents of selected candidates will be verified at the time of Interview, and in the event of any information mentioned in application/CV/testimonials found false or incorrect, their candidature straightway shall be cancelled.
7. No TA/DA will be paid for attending the interview/test.
8. For any queries regarding the position, please email Dr. Abhishek Acharya at abhishek@eced.svnit.ac.in.

s/d
Director